

BrightnESS

**Building a research infrastructure and synergies for highest scientific impact
on ESS**

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brightness

Deliverable Report: D4.9 – Detector electronics chain



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3 List of Abbreviations

| | |
|-------|--|
| ADC | Analog-to-digital converter |
| ASIC | Application-specific integrated circuit |
| ATLAS | ATLAS Experiment at CERN |
| CMOS | Complementary metal-oxide-semiconductor |
| ESS | European Spallation Source |
| FEC | Front-End Concentrator |
| FPGA | Field-programmable gate array |
| Gd | Gadolinium |
| GEM | Gaseous Electron Multiplier |
| IFE | Institute for Energy Technology, Norway |
| LDO | Low Dropout Regulators |
| LVDS | Low-voltage differential signalling |
| NMX | Macromolecular crystallography diffractometer to be installed at the ESS |
| PCI | Peripheral Component Interconnect |
| SoC | System on a Chip |
| SRIO | Serial Rapid Input-Output |
| SRS | Scalable Readout System |
| SRU | Scalable Readout Unit |
| TPC | Time Projection Chamber |
| VFAT | Virtual file allocation table |
| VMM | Virtual Machine Manager |

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6 Executive Summary

This deliverable report *D4.9 – Detector electronics chain* describes the completion of a readout electronics chain for the NMX prototype detector, currently developed jointly by ESS and CERN within Work Package 4 Task 4.1.

It contains information about the already available hardware used as a starting point for dedicated developments and the reasons why these components were selected. The components are in particular the VMM front-end ASIC developed within the ATLAS New Small Wheel upgrade project and the Scalable Readout System of the RD51 Collaboration¹.

The VMM ASIC features high readout rates, low electronic noise, excellent configuration possibilities and easy availability. The Scalable Readout System (SRS) is also freely available and allows for the implementation of new front-end ASICs within the timescale of this project. Moreover, as the name suggests, this readout system can be scaled from small detectors used during the development phase to the final prototype (to be delivered at the end of the project), or even several and larger detectors like foreseen at the NMX instrument.

Several new hardware components and FPGA firmware have been developed in order to implement the VMM Application Specific Integrated Circuit (ASIC) into the Scalable Readout System. The system shows reliable operation in laboratory tests as well as in a first test beam at the R2D2 beamline at IFE, Norway.

Towards the end of the BrightnESS project, improvements to the system will be implemented to increase the readout rate and provide a user-friendly system with online data monitoring. It should be noted that there is close collaborative work between BrightnESS WP4 and WP5 on this online data monitoring.

7 Report on Implementation Process and Status of Deliverable

The readout electronics is a key component of the NMX prototype detector. The NMX detector concept consists of a Gaseous Electron Multiplier (GEM) (Sauli, 1996) with Gadolinium converter. This neutron detector uses the micro Time Projection Chamber (μ TPC) analysis method in order to improve the spatial resolution to meet the requirements of the final NMX instrument. Moreover, the detector electronics chain aims to achieve readout rates comparable to those of at the final instrument, taking into account the rates of neutrons at the instrument and the high detection efficiency of the upgraded NMX instrument with enriched Gadolinium.

The detailed detector concept is as follows (see Figure 1):

Neutrons scattering off the sample will first penetrate the thin detector structure before they interact with the neutron converter consisting of a Gadolinium sheet at the cathode. One electron is released into the gas volume inside the detector with enough energy to ionise gas molecules along its path. The electrons of the ionisation are drifted towards the GEM stack in the electric field between the cathode and the top GEM. In the GEM structure, these electrons are multiplied, such that at the bottom of the GEM stack a measurable amount of charge is released, which is collected by a segmented anode in order to obtain spatial resolution. The anode is realised as an x-y grid of anode strips with 400 μ m pitch. The strips are connected to a charge sensitive Application Specific Integrated Circuit (ASIC) that provides information about the charge signal, as for example the arrival time.

The path of the conversion electron can be reconstructed in 3D by using the x-y information of the anode strips and the arrival time of the charge at the anode like in a TPC. The starting point of the track is the impact point of the neutron in the Gadolinium cathode.

¹ See: <http://rd51-public.web.cern.ch/rd51-public/>

It has been shown (Pfeiffer & Thuiner, 2016), that an impact position resolution better than 350 μm can be achieved, which meets the requirements of the NMX instrument. The measurements leading to this result have been obtained with small scale versions of the prototype detector being developed within this BrightnESS subtask and a pre-version of detector electronics.

Besides the detector itself, a new detector electronics chain was developed. Different possibilities of existing systems were evaluated in order to be able to start from already existing technology which can be adapted for the specific needs of the NMX instrument. The chosen hardware components are introduced in detail in Sections 8.1 and 8.2.

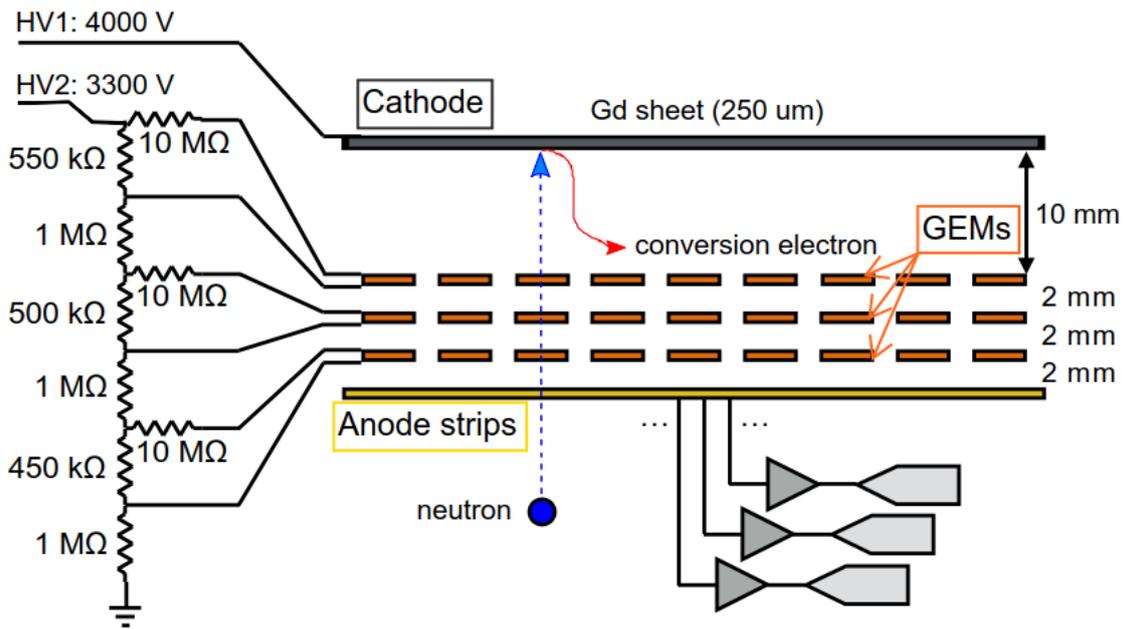


Figure 1: Sketch of the NMX prototype detector concept

The Virtual Machine Manager (VMM) ASIC developed by Brookhaven National Laboratory within the ATALS New Small Wheel upgrade project is the ideal candidate to handle the expected signal rates at the NMX instrument. Other front-end ASICs like VFAT (Virtual File Allocation Table) could not fulfil all the requirements.

As a starting point for the NMX prototype readout, the Scalable Readout System of the RD51 collaboration has been chosen. It allows for the implementation of new front-end ASICs without the need to develop a completely new system. Due to its flexibility, the development of a readout chain for the prototype detector was feasible within the timescale of the BrightnESS project.

At the time of the due date of this deliverable, the complete readout chain is functional. The VMM has been implemented in the SRS by developing dedicated FPGA firmware and hardware components. The system has been used during a test beam at the R2D2 beamline at IFE, Norway, to read out a small version of the NMX prototype to be delivered at the end of this project.

Ongoing activities include optimisations of the system and upscaling activities in order to read out the final prototype. In addition, upgrade possibilities for the current SRS hardware are evaluated to achieve even higher readout rates.

The implementation of the VMM in the scalable readout system has triggered interest by several research teams in different research fields to use the electronics chain as readout for their particular experiment.

8 Technical Content

8.1 The Scalable Readout System (SRS)

With the Scalable Readout System (SRS) (S. Martoiu et al., 2013), the RD51 Collaboration at CERN has developed a versatile multi-purpose readout system that can be scaled up from small detectors with only a few readout channels to large LHC-like experiments. It can be adapted to different front-end ASICs by only exchanging part of the hardware components.

Figure 2 shows a schematic view of the system. On the detector side, it consists of the hybrids, which hold the user specific front end ASICs. Those hybrids are connected to an adapter card which also is user-specific and connects via PCI to the core of the SRS common part: the Front-End Concentrator (FEC) card. This card holds among others a Virtex 6 FPGA, a Gigabit Ethernet SFP connector, DDR3 and flash memory. Up to eight FECs can be housed in a Eurocrate, from which the power is provided by an ATX power supply. Towards the computer with data acquisition and slow control software, the data from several FECs can be combined by a Scalable Readout Unit (SRU) or a Gigabit Ethernet switch. The first SRS FECs (version 3) became available in 2010, while the current version 6 is available since 2013. In order to implement a new front end ASIC into SRS, hybrids and the adapter card have to be designed and a dedicated FPGA firmware has to be developed.

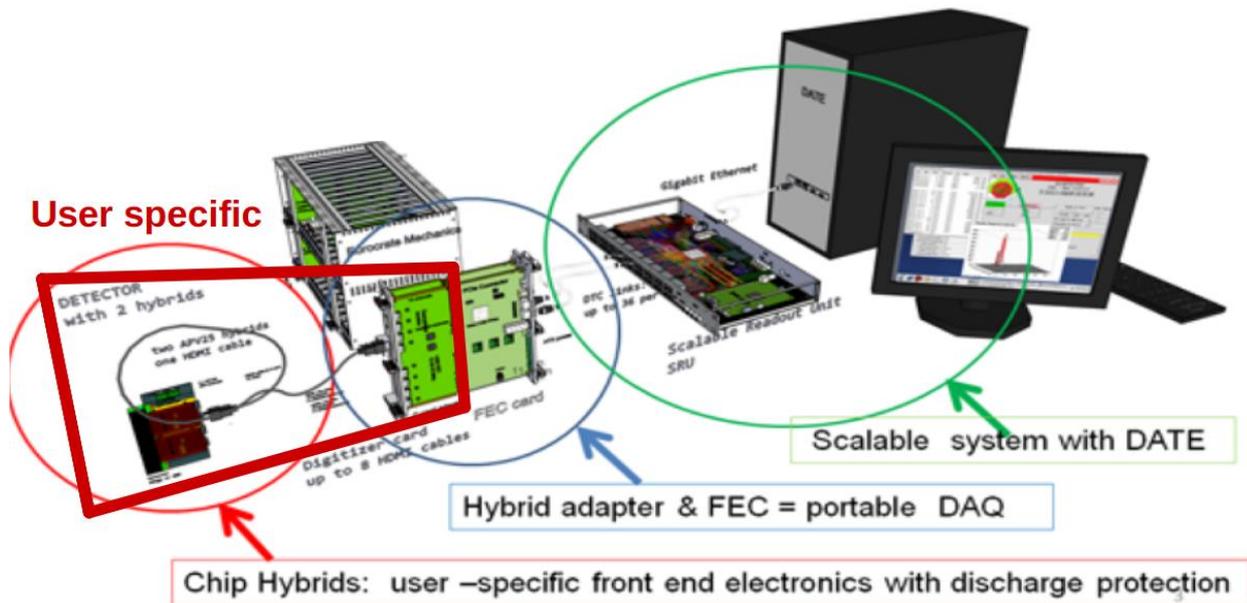


Figure 2: Schematic view of the SRS

8.2 The VMM ASIC

For the ATLAS New Small Wheel upgrade project, a new front end ASIC, the VMM (De Geronimo, et al., 2013) has been designed. The ASIC is produced in 130 nm CMOS technology and the latest version 3 was delivered at the end of 2016. It is configured via two single ended lines (clock and data).

The VMM has 64 charge sensitive input channels, where every channel holds a charge amplifier, shaper and digitisation logic. Test pulses for calibration can be applied to every individual channel. In



the mode of operation interesting for the application in this project, the output of the chip is digital information about the pulse amplitude (10 bit), arrival time (20 bit) the channel hit (6 bit). In addition, there is an over-threshold indicator bit and a hit flag, such that the information about a signal in one input channel results in a total of 38 bit. The digitisation procedure is displayed in Figure 3.

The electronic noise of the ASIC has been measured to be in the order of 100 – 200 electrons for low input capacitances.

In case a signal from the detector, noise or a test pulse is over the channel threshold, the amplitude at the peak is measured and converted by the 10 bit analog-to-digital converter (ADC). The time information consists of two parts. A low precession time information of 12 bit is provided by a counter operated at a selectable clock frequency. For a more precise timing, a voltage is continuously ramped up at the time of the peak until the next clock edge. The amplitude of the voltage is converted by an 8 bit ADC, which provides the precise time information (down to 0.5 nanosecond). Instead of the timing at the peak, also the time at threshold can be used. Besides this option, a numerous settings can be applied globally to the VMM like the ramp speed (mV/ns), gain (mV/fC), threshold, test pulse amplitude or shaping time and locally to every channel individually like threshold trim, masking or test pulse enable. For more details, the reader is referred to the VMM user manual, which will be provided with the system.

The ASIC will be available without export restrictions and can be ordered together with the productions for the ATLAS upgrade project due to a close collaboration with the developers.

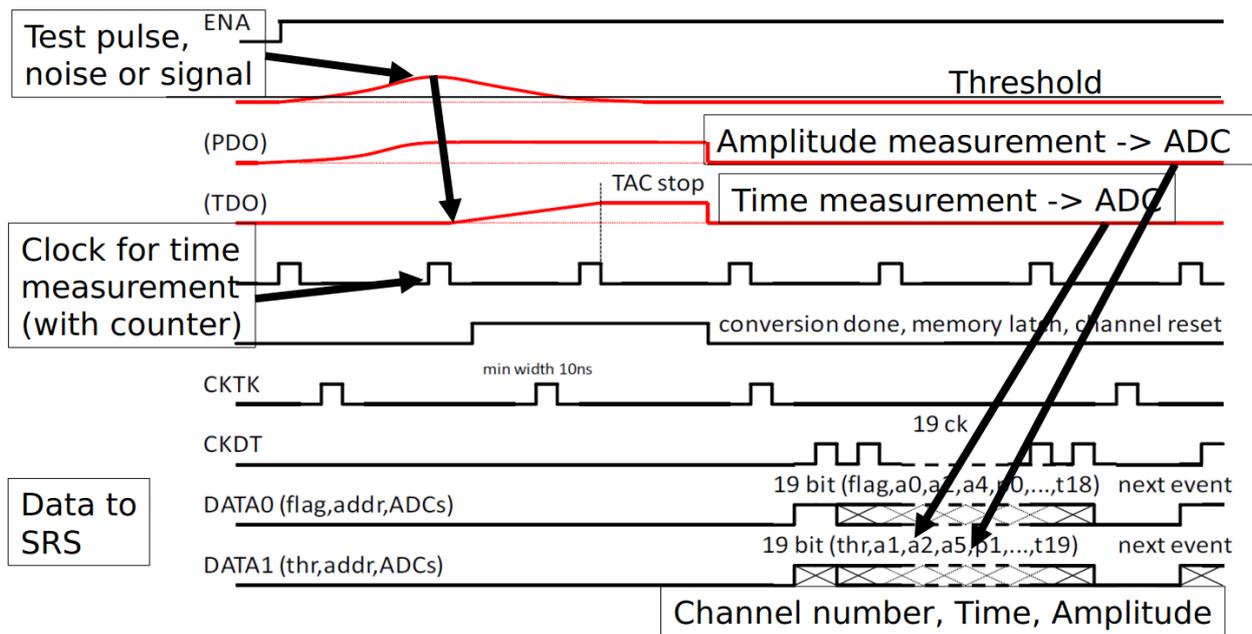


Figure 3: Digitisation procedure of the VMM ASIC

8.3 Implementation of the VMM in SRS

In order to implement the VMM in the SRS, FPGA firmware, an adapter card and a VMM hybrid have been developed.

Figure 4 shows the SRS FEC on the left connected to the adapter card for the VMM called DCard (digital card, as the data from the VMM is purely digital). The PCB holds mainly LVDS drivers to transmit the clock and configuration data to the VMM hybrids, of which eight can be connected via HDMI to one single DCard. This card can also provide power to a lower quantity of hybrids for testing. In case more hybrids are connected, they are powered by an external supply.



Figure 4: SRS FECv6 with DCard

Two VMM ASICs are wire bonded onto one VMM hybrid, as can be seen in Figure 5, such that the hybrid can read out 128 detector channels. On the left part of the hybrid, the connector to the detector is placed together with protection circuits against too high charge due to sparks. In order to combine the data from the two ASICs and to configure them, a Spartan 6 FPGA is also implemented on the hybrid, which also holds Low Dropout Regulators (LDOs) for a stable power supply and a flash memory. The size of a hybrid is 5 cm by 8 cm.

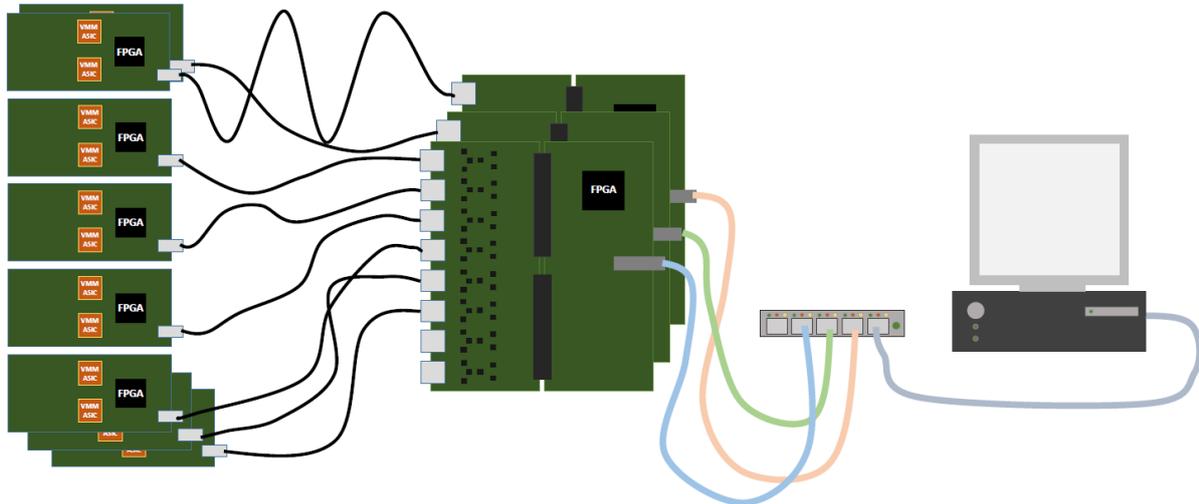


Figure 5: VMM hybrid

For the Spartan 6 FPGA on the hybrid as well as for the Virtex 6 FPGA on the FEC, new firmware has been developed to control and read out the VMM.

8.4 Readout chain

The detector electronics chain is shown in a schematic overview in Figure 6. It starts on the detector side in the left part of the image with the VMM hybrids. They are connected via HDMI cables to the DCard + FEC. Several FECs are connected with an Ethernet switch to the computer.



VMM Hybrid → HDMI cable → Adapter card + FEC → Ethernet → Switch → Ethernet → PC

Figure 6: Schematic view of the detector electronics chain (components not to scale)

Figure 7 shows a screenshot of the data arriving at the computer recorded with the Wireshark tool. In the top part, the different Ethernet network packages are shown, which are interchanged between the FEC under test and the computer with slow control and data acquisition software. In the lower part, the content of one of the data packages is shown. A Wireshark plugin is used to display the binary content in a human readable way. The data consists of a header with a frame counter, data ID, VMM ID and a time stamp provided by the SRS followed by the hits that particular VMM (in this case VMM 0, which is one of the two VMMs on a hybrid connected to channel 0 on the adapter card) has registered. For each individual hit, the channel, coarse time (bcid), precise time (tdc) and amplitude (adc) of the hit is shown. In this view, the over-threshold flag is not displayed.

In order to decrease the amount of expensive hardware components (FEC and DCard) the possibility to connect more than eight hybrids per FEC is evaluated.

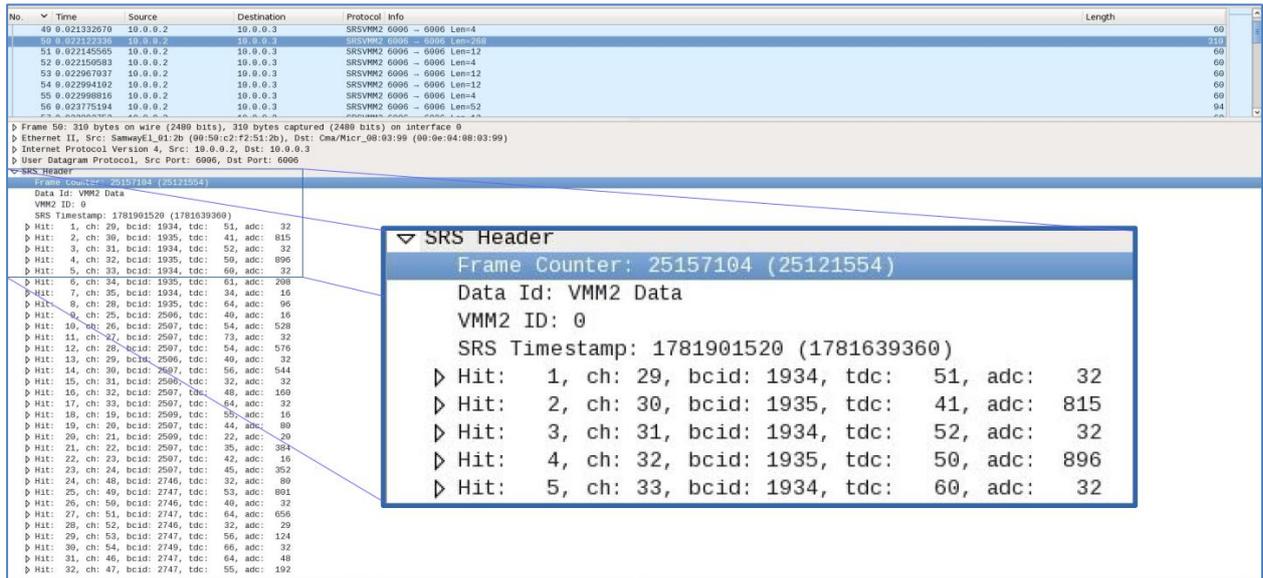


Figure 7: Wireshark network analyser screenshot showing the data received from the readout system via Ethernet

8.5 The VMM readout challenge

The readout of the VMM is challenging for any readout system, as the ASIC is self-triggered. This means that whenever a charge signal is over threshold in one of the channels of the chip, the VMM will write the information on that hit as defined by the settings. Each VMM channel has a readout threshold. These thresholds have to be set low enough so that the channels record all valuable data, and high enough to stop the channels from acquiring too much noise. The readout system is capable of reading out the data from the VMM with at least the expected hit rate of the detector. In the following subsections, these aspects will be addressed with respect to the expectations at the NMX instrument.

8.5.1 Maximum data rates of the ASIC

Each VMM channel can handle a hit rate of at most 4 MHits/s and for each hit, 38 bit of data are generated. However, it is not possible to read out such large amounts of data in case all 64 channels of the VMM receive that hit rate continuously. The maximum readout clock of the VMM is 200 MHz and the data can be read out on two data lines in double data rate, which results in a maximum readout rate of 800 Mbit/s or 21 MHits/s. In order to handle high hit rates for a short time (like in collisions of particle physics experiments, for which the VMM was designed) there is a four-hit deep buffer for every channel, which can be extended with an additional 64 hit deep buffer in a specific readout mode. However, this mode might not be useful for the beam structure at NMX. Since at NMX the neutron rate is more or less continuous, only the 4 hit deep buffer can be used. Hence, the readout system has to be capable to read out the VMM continuously with a higher speed than the expected hit rate.

8.5.2 Expected rates at NMX

To calculate the expected rates of the NMX instrument, very conservative assumptions and worst-case scenarios have been taken into account. Therefore, the actual hit rate in the real experiment will always be lower than the calculated ones.



The time averaged expected neutron rate n of the beam at NMX is $4.8 \cdot 10^8$ n/s on a sample of at most 5 mm \times 5 mm. 2% of the neutrons or $9.6 \cdot 10^6$ n/s will scatter into whole 4π solid angle. The detectors at their position closest to the target cover one sixth of the solid angle, such that they receive at most $1.6 \cdot 10^6$ n/s. As one detector will have an active area of 2621.44 cm² the rate per area is $6.104 \cdot 10^2$ n/s/cm². Assuming a conversion efficiency of neutrons on the gadolinium (upgraded detector with enriched ¹⁵⁷Gd taken into account) of 35 %, the number of conversion electrons e^- is $2.136 \cdot 10^2$ e^- /s/cm². These electrons will leave a track in the drift region of the detector and induce a signal on not more than 20 readout strips. Each strip covers exactly 1 cm². Hence, the hit rate for the strips is $4.272 \cdot 10^3$ Hz. Each strip is read out by one input channel of the VMM and a hit is converted to 38 bits of data resulting in an average data rate per channel of $1.623 \cdot 10^5$ bit/s. As one VMM has 64 channels, the average data rate per ASIC is $1.039 \cdot 10^7$ bit/s or 10.39 Mbit/s.

Notes:

1. The diffraction pattern contains spots, in which far more than the average 2 % of the neutrons are scattered. However, as the conversion electrons from the neutrons are distributed over at most 20 strips, the higher hit rate is smeared out on the readout and the average hit rate can be used for the calculations. The spots are then reconstructed within the μ TPC analysis.
2. The beam rate on which the calculations are based on is a time averaged rate. However, the ESS accelerator delivers pulses of 4 ms length with 14 Hz repetition rate resulting in a factor 18 higher instantaneous rates. However, due to the different wavelengths of the neutrons from the target and sample, the pulses are widened to about 71 ms, such that a continuous beam of neutrons (of different wavelength) arrives at the sample. The intensity distribution of those neutrons depends on the wavelength distribution from the target and sample.
3. The gamma induced background, which also induces signals on the strips has not been simulated so far. It will significantly contribute to the average data rate and could add a factor up to 10%. A factor of many is no problem here.
4. In case of very short exceedances of the average rate by several orders of magnitude, the four-hit deep buffer of every VMM channel can extenuate the data rate. For longer exceedances of the average rate by only a few orders of magnitude, the Spartan 6 FPGA data buffer lowers the data rate to the SRS.

Due to the gamma background, the maximum average data rate from one VMM is expected to be less than 100 Mbit/s, which is well below the maximum readout rate of 800 Mbit/s.

8.5.3 Capabilities of the current SRS hardware

The hardware of the SRS system has not been designed for a particular application at the NMX instrument. The aim of using this system is to provide a readout for the prototype detector for NMX. Thus, the hardware does not necessarily need to provide capabilities to read out the prototype at the expected rates for the final NMX instrument. Upgrades to the SRS could enable the system to be also used at the final experiment. However, as will be pointed out in this section, most of the hardware components already meet the requirements for data rates as expected in the final experiment.

As explained above, the VMM can provide a maximum data rate of 800 Mbit/s in case it is read out by a 200 MHz clock. The global clock tree of the Spartan 6 FPGA (speed grade -2) is capable of providing clock speeds up to 375 MHz and the serial transmitters can send out data up to 950 Mbit/s (Xilinx Inc, 2015).



The link between the hybrid with the Spartan 6 FPGA and the DCard connected to the FEC with the Vertex 6 FPGA is realised by HDMI cables. The Cat2 HDMI cables are tested at 340 MHz and can be reliably operated up to 825 MHz clock frequencies.

The Virtex 6 FPGA (speed grade -1) on the FEC has a global clock tree that is specified up to 645 MHz and has input receivers for up to 1100 MHz (Xilinx Inc, 2014). Up to this part of the readout chain, the maximum data rate the VMM provides can be handled by the current hardware. For transmission of the data to the computer, however, the Virtex 6 FPGA on the FEC can only provide Gigabit Ethernet. This bandwidth would still be sufficient to read out one VMM at maximum speed. However, there are already two VMMs on one hybrid and eight to sixteen hybrids can be connected to one FEC. As calculated in the previous section, the maximum average rate per VMM is 100 Mbit/s. Given this rate, only ten VMMs or five hybrids could be read out per SRS FEC.

For testing of the NMX prototype detectors, where the neutron rate will be significantly lower than at the ESS, the current FEC can still be used. For an application at the final NMX instrument, additional developments are necessary.

There are several options to overcome the bottleneck caused by the Gigabit Ethernet link between FEC and Computer:

1. reduce the data to be transmitted to the computer by an implementation of analysis algorithms in the FPGA firmware (as the signal of one neutron is spread on 20 strips, a data reduction of a factor of 20 can be achieved in case μ TPC algorithms to find the impact point would be implemented);
2. develop an adapter board with SRIO (up to 8 Gbit/s) for the FEC;
3. develop a new FEC version with 10 or 100 Gigabit Ethernet;
4. replace the FEC by different hardware capable to transmit larger amounts of data.

8.6 Studies on SRS upgrade

An SRS upgrade option using a Texas Instruments evaluation board (EVMK2H) with SOC56r (system on chip) is currently being studied. To circumvent the 1 Gbit/s ethernet limitation of the FEC output, the two SFP ports of the FEC could be used instead to transmit the data with 2 x 5 GB/s via optical SRIO (Serial Rapid IO) to a microTCA crate with the EVMK2H. This evaluation board supports SRIO and 10 Gbit Ethernet, and has eight TMS320C66x DSP and four Cortex A15 ARM cores. The μ TCP algorithm can be carried out on these cores, which would reduce the amount of data by a factor of 20. Subsequently the reduced data can then be sent out via 10Gbit Ethernet to the PC.



Figure 8:Ti EVMK2H with SoC, SRIO and 10 Gbit ethernet

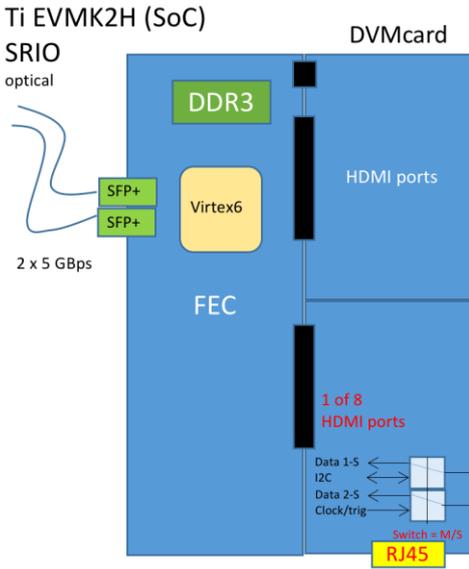


Figure 9: Upgrade of FEC using optical SRIO

9 Conclusion

The VMM ASIC has been implemented in the SRS. The established detector electronics chain provides a powerful, high speed readout system able to read out charge sensitive detectors of a range even wider than the application at the NMX prototype and the final instrument. This has triggered interest in the system also by groups outside the neutron detector community.

For the implementation of the VMM in SRS, new hardware components have been developed. On the detector side, hybrids hold two VMM ASICs which are connected by a discharge protection circuit to the anode strips of the detector. A Spartan 6 FPGA concentrates the data, simplifies the configuration and establishes a link via HDMI cables to the adapter card connected to the SRS common FEC card. This card can connect up to eight hybrids or even more in an upgraded version. The Virtex 6 FPGA concentrates all the data and provides the Gigabit Ethernet protocol to communicate with standard network components and the computer, where the control and data taking software is executed. The system still has enough flexibility to introduce further upgrades. The current version meets the requirements for tests of the NMX prototype to be developed within the BrightnESS project. For an application at the final NMX instrument at ESS, the system can be applied directly with an increase in components or more advanced upgrades.

The current version of the detector electronics chain has been used in laboratory tests and a test beam and has showed reliable performance. The capabilities of the system will continue to be improved in the remaining time of the BrightnESS project. Currently, the system is scaled up in order to read out the final prototype detector during test beam campaigns with the aim to evaluate the performance of the developed detector concept.



10 List of Publications

- D. Pfeiffer, F. Resnati, J. Birch, M. Etxegarai, R. Hall-Wilton, C. Höglund, L. Hultman, I. Llamas-Jansa, E. Oliveri, E. Oksanen, L. Robinson, L. Ropelewski, S. Schmidt, C. Strelj, P. Thuiner. "[First Measurements with New High-Resolution Gadolinium-GEM Neutron Detectors](#)", *Journal of Instrumentation* 11, P05011 (2016); [doi:10.1088/1748-0221/11/05/P05011](https://doi.org/10.1088/1748-0221/11/05/P05011); [arXiv:1510.02365v4](https://arxiv.org/abs/1510.02365v4).
- D. Pfeiffer, F. Resnati, J. Birch, R. Hall-Wilton, C. Höglund, L. Hultman, G. Iakovidis, E. Oliveri, E. Oksanen, L. Ropelewski, P. Thuiner. "The μ TPC Method: Improving the Position Resolution of Neutron Detectors Based on MPGDs", *Journal of Instrumentation* 10, P04004 (2015); [doi:10.1088/1748-0221/10/04/P04004](https://doi.org/10.1088/1748-0221/10/04/P04004); [arXiv:1501.05022v1](https://arxiv.org/abs/1501.05022v1).

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